REMARKS

Upon entry of this Amendment, claims 29-48 are pending. Claims 29 and 39 are amended and claims 38 and 48 are cancelled.

In the April 28, 2006 Office Action, the examiner:

- rejected claims 29, 30, 32-40 and 42-48 under 35 U.S.C. § 102(e) as anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as obvious over, U.S. Patent Application Publication No. 2002/0033504 to Ohnakado ("the Ohnakado publication");
- rejected claims 29-48 under 35 U.S.C. § 103(a) as unpatentable over the Ohnakado publication in view of U.S. Patent No. 5,741,740 to Jang ("the Jang patent");
- rejected claims 29, 30, 32-40 and 42-48 under 35 U.S.C. § 102(e) as anticipated by, or in the alternative, under 35 U.S.C. § 103(a), as obvious over, U.S. Patent No. 5,674,761 to Chang et al. ("the Chang patent"); and
- rejected claims 29-48 under 35 U.S.C. § 103(a) as unpatentable over the Ohnakado publication in view of the Jang patent, and further in view of U.S. Patent No. 4,646,427 to Doyle ("the Doyle patent").

Rejections

Claims 29-48 stand variously rejected as anticipated by, or obvious over the Ohnakado publication; the Ohnakado publication in view of the Jang patent; the Chang patent; and the Ohnakado publication in view of the Jang and Doyle patents.

Claim 29 has been amended to recite, *inter alia*:

> ". . . first and second power supply voltage sources . . .
> a plurality of serially connected polycrystalline silicon diodes . . .
> wherein the plurality of serially connected polycrystalline silicon diodes comprises "n" diodes, and the number "n" is determined by the formula:
> $n >= (V_{noise} + |Vx1-Vx2|)/ V_T$
> where:
> n is the number of serially connected polycrystalline silicon diodes,

V_{noise} is the maximum voltage level difference allowed to be present on the internal integrated circuit located between the first power supply voltage source and the second power supply voltage source,
Vx1 is the magnitude of the first power supply voltage source,
Vx2 is the magnitude of the second power supply voltage source, and
V_T is the threshold voltage of each of the polycrystalline silicon diodes."

Claim 39 has been amended to recite, *inter alia,*

". . . first and second power supply voltage sources . . .
an internal circuit connected between the first and second power distribution networks; and . . .
a plurality of serially connected polycrystalline silicon diodes . . .
wherein the plurality of serially connected polycrystalline silicon diodes comprises "n" diodes, and the number "n" is determined by the formula:
$n >= (V_{noise} + |Vx1-Vx2|)/ V_T$
where:
n is the number of serially connected polycrystalline silicon diodes,
V_{noise} is the maximum voltage level difference allowed to be present on the internal integrated circuit located between the first power supply voltage source and the second power supply voltage source,
Vx1 is the magnitude of the first power supply voltage source,
Vx2 is the magnitude of the second power supply voltage source, and
V_T is the threshold voltage of each of the polycrystalline silicon diodes."

Claims 29 and 39 are not anticipated by any of the references cited by the examiner, nor are they rendered obvious by any of the references when taken alone or in combination. Specifically, none of the cited references disclose, either expressly or inherently, the arrangement of diodes according by the formula recited in claims 29 and 39.

In the Office Action mailed September 27, 2006, the examiner stated:

"the claim recitations do not specifically recite any specific magnitudes or values for threshold voltages, noise voltages, supply voltages, or number of diodes which would unequivocally distinguish over the applied are values or magnitudes. At best the recited language can be equated to 'predetermined' magnitudes which would in no way structurally distinguish over the inherent values of the applied art. In other words, applicant has not shown that the applied art does not also inherently possess the claimed 'n' number of diodes, 'noise voltage,' 'threshold voltage,' etc."

(*See* Office Action mailed 9/27/06, pg. 4, lines 7-15.)

But contrary to the examiner's assertion, the limitations are not equatable with "predetermined" values or magnitudes. Rather, the claim limitations recite specific structural relationships between device elements. These relationships are based on specifically delineated and recited properties of the device elements which represent a *structural difference* between the claimed invention and the prior art.

The examiner further states that "applicant has not shown that the applied art does not also inherently possess the claimed 'n' number of diodes, 'noise voltage,' 'threshold voltage,' etc." (*See id.*) But the initial burden of proving inherency is on the examiner, not the applicant. "In relying on a theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *See ex parte Levy,* 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). The examiner has not met this initial burden to show the features are inherently disclosed in any of the cited references.

Furthermore, the Court of Appeals for the Federal Circuit has stated that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *See in re Rijckaert,* 9 F.3d 1531 (Fed. Cir. 1993). Further, "[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *See In re Robertson*, 169 F.3d 743, 754 (Fed. Cir. 1999).

None of the references cited by the examiner in rejecting claims 38 and 48 disclose, either expressly or inherently, the structural arrangement of diodes in the manner described by the formula recited in claims 29 and 39. Applicants thus request that the rejections of claims 29 and 39 be withdrawn, and that these claims be allowed. With respect to claims 30-37 and 40-47, which depend from claims 29 and 39 and recite additional features of the invention, applicant requests that the rejections of these claims be withdrawn and that these claims be allowed for the same reasons as stated for claims 29 and 39.

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Applicants submit that this application is in condition for allowance. Early notification to that effect is respectfully requested. If a telephone conference would be of assistance in advancing prosecution of the above-captioned application, the examiner is invited to call the undersigned attorney at **(609) 631-2491**.

A fee of **$790** is believed due for the Request for Continued Examination which is being submitted with this response. The Commissioner for Patents is hereby authorized to charge this fee, as well as any other required fees, to deposit account **04-1679.**

Respectfully submitted,

Dated: December 15, 2006

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